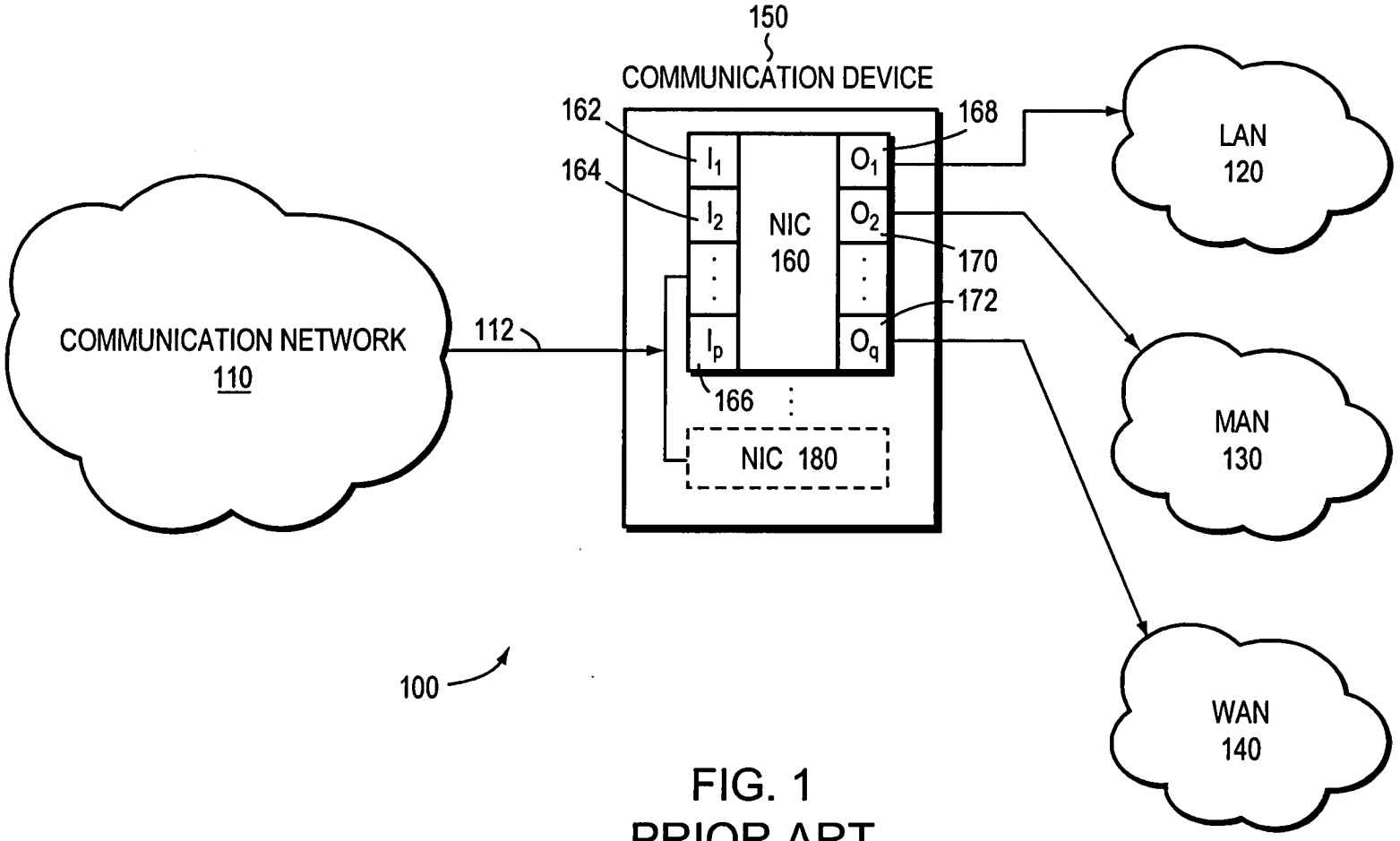

FIG. 1
PRIOR ART

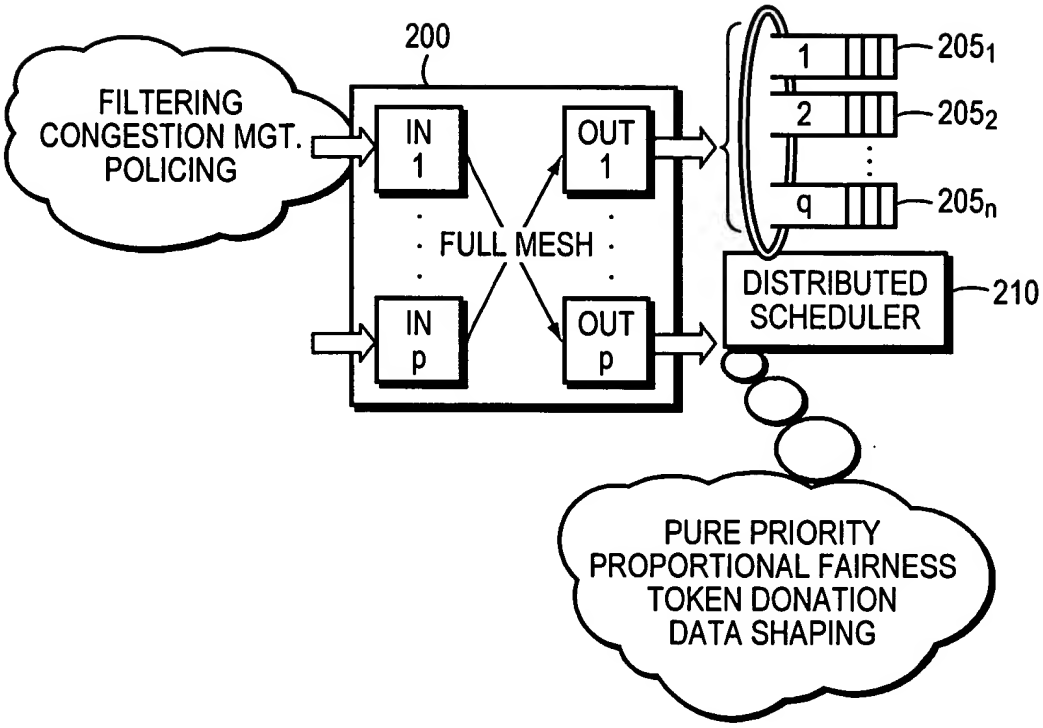

FIG. 2A
PRIOR ART

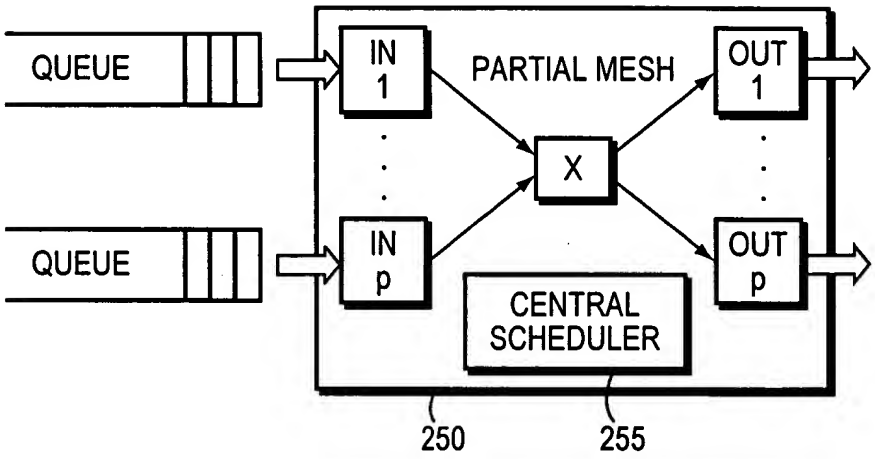

FIG. 2B
PRIOR ART

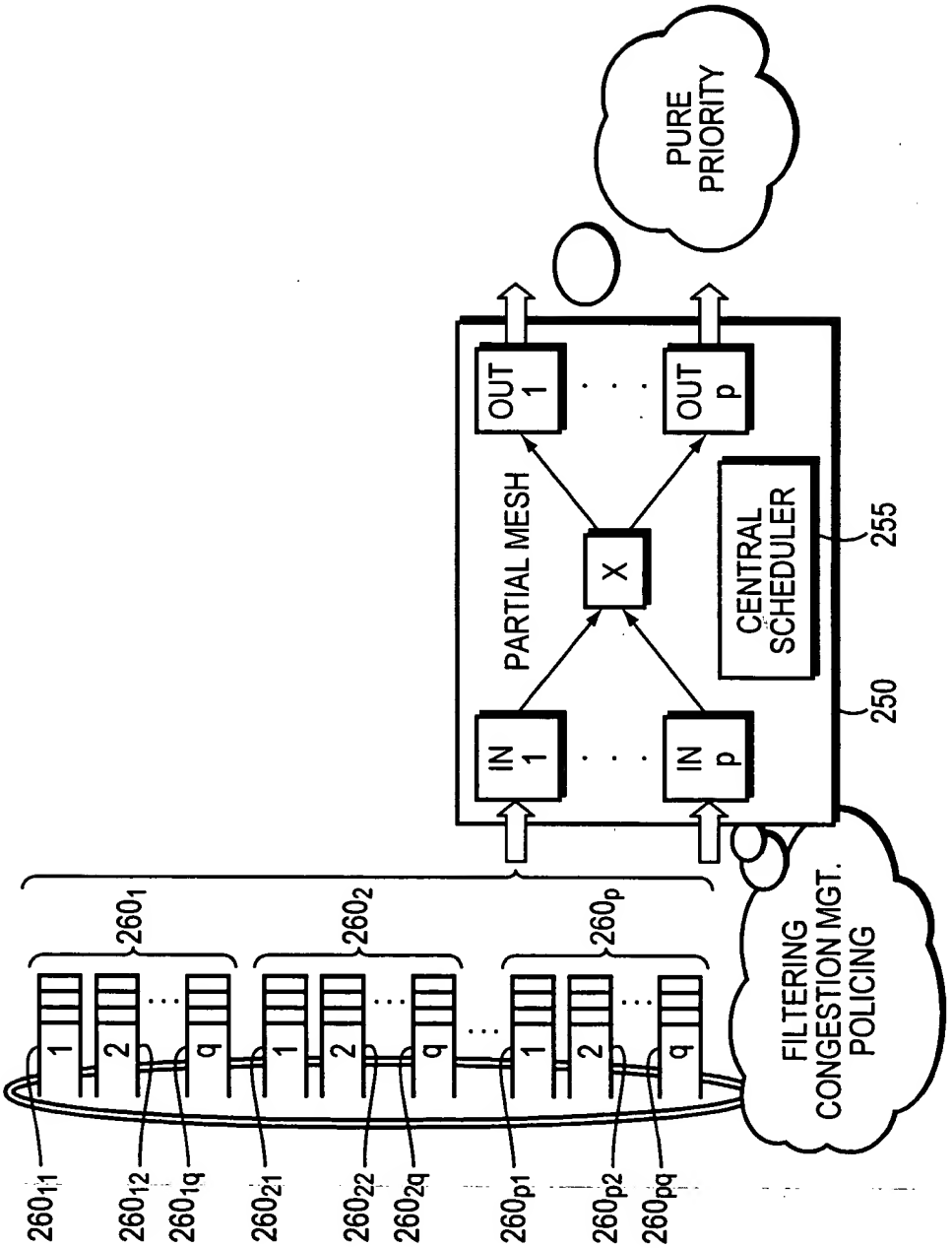

FIG. 2C
PRIOR ART

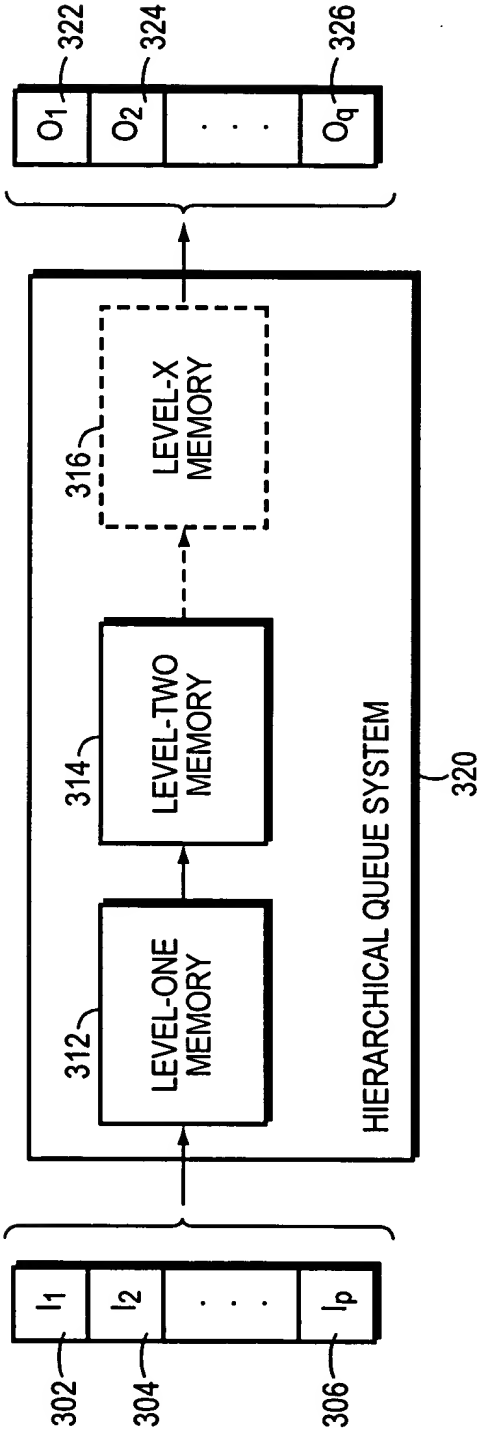
I_1
I_2
I_p
302
304
306
LEVEL-ONE MEMORY
312
LEVEL-TWO MEMORY
314
LEVEL-X MEMORY
316
HIERARCHICAL QUEUE SYSTEM
320
O_1
O_2
O_q
322
324
326

FIG. 3A

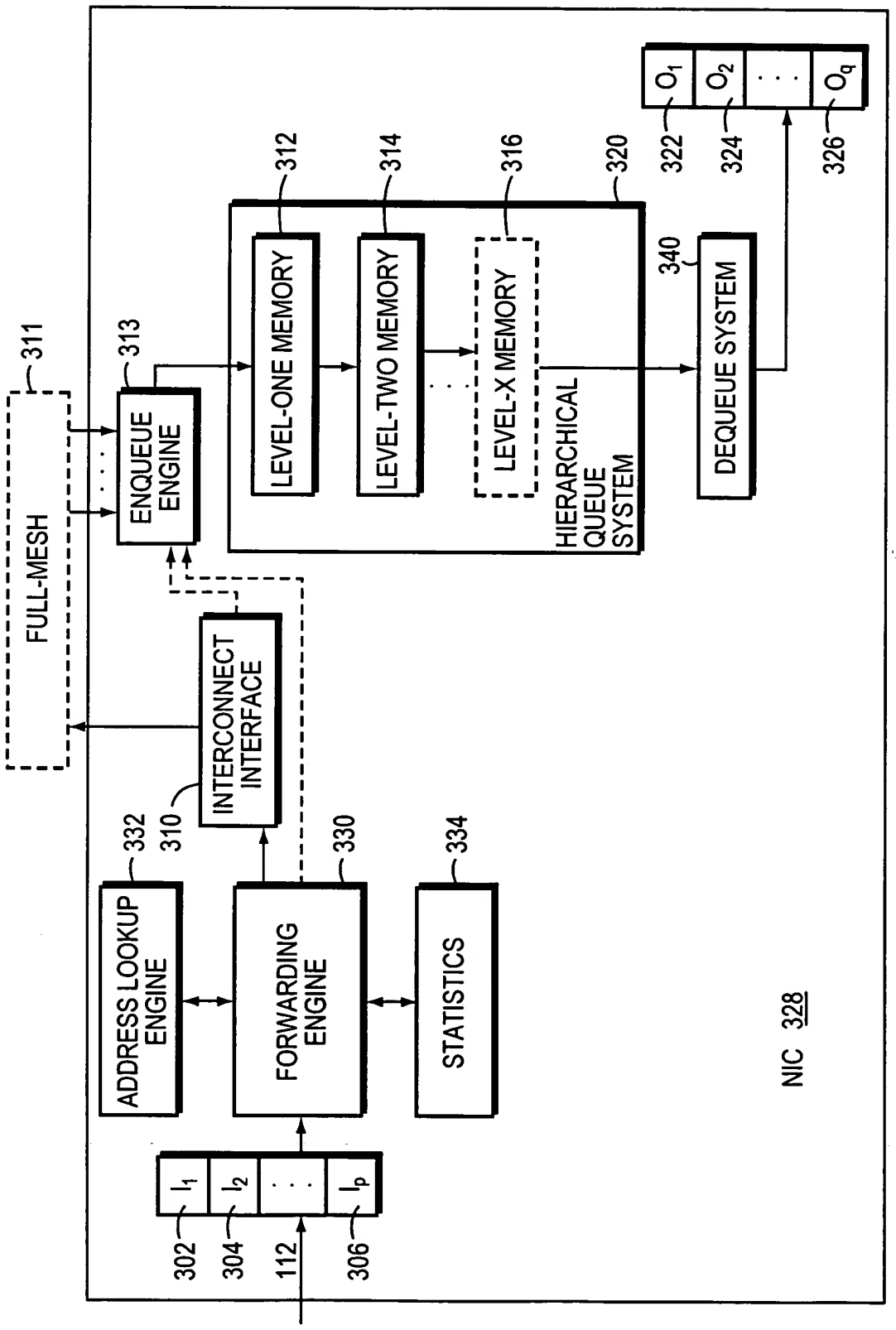
NIC 328
ADDRESS LOOKUP ENGINE
FORWARDING ENGINE
STATISTICS
INTERCONNECT INTERFACE
ENQUEUE ENGINE
FULL-MESH
LEVEL-ONE MEMORY
LEVEL-TWO MEMORY
LEVEL-X MEMORY
HIERARCHICAL QUEUE SYSTEM
DEQUEUE SYSTEM
I_1
I_2
I_p
O_1
O_2
O_q
302
304
306
310
311
312
313
314
316
320
322
324
326
330
332
334
340
112

FIG. 3B

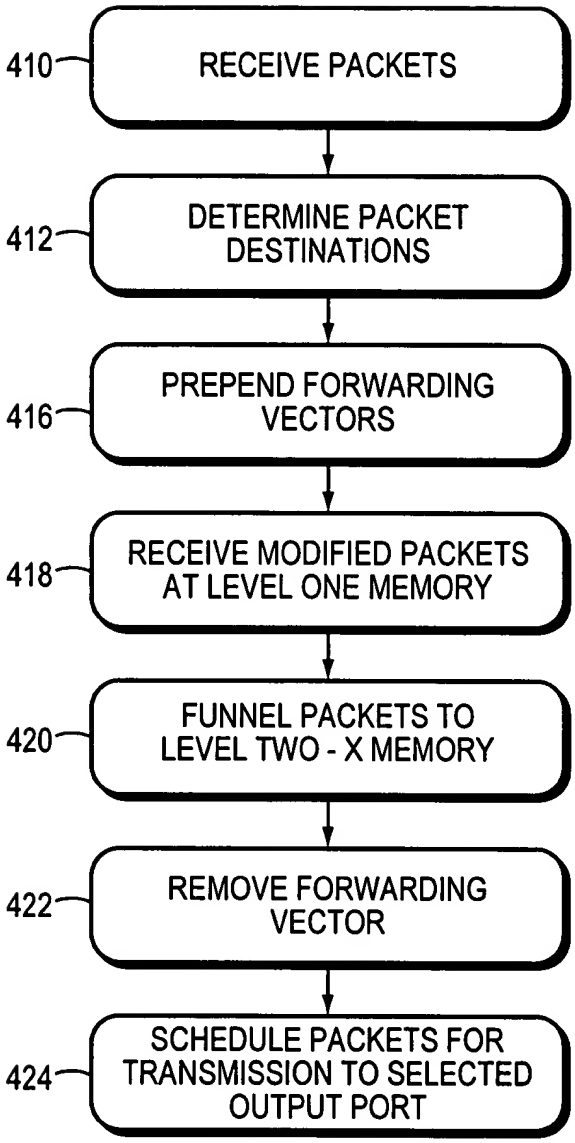
410
RECEIVE PACKETS
412
DETERMINE PACKET DESTINATIONS
416
PREPEND FORWARDING VECTORS
418
RECEIVE MODIFIED PACKETS AT LEVEL ONE MEMORY
420
FUNNEL PACKETS TO LEVEL TWO - X MEMORY
422
REMOVE FORWARDING VECTOR
424
SCHEDULE PACKETS FOR TRANSMISSION TO SELECTED OUTPUT PORT

FIG. 4

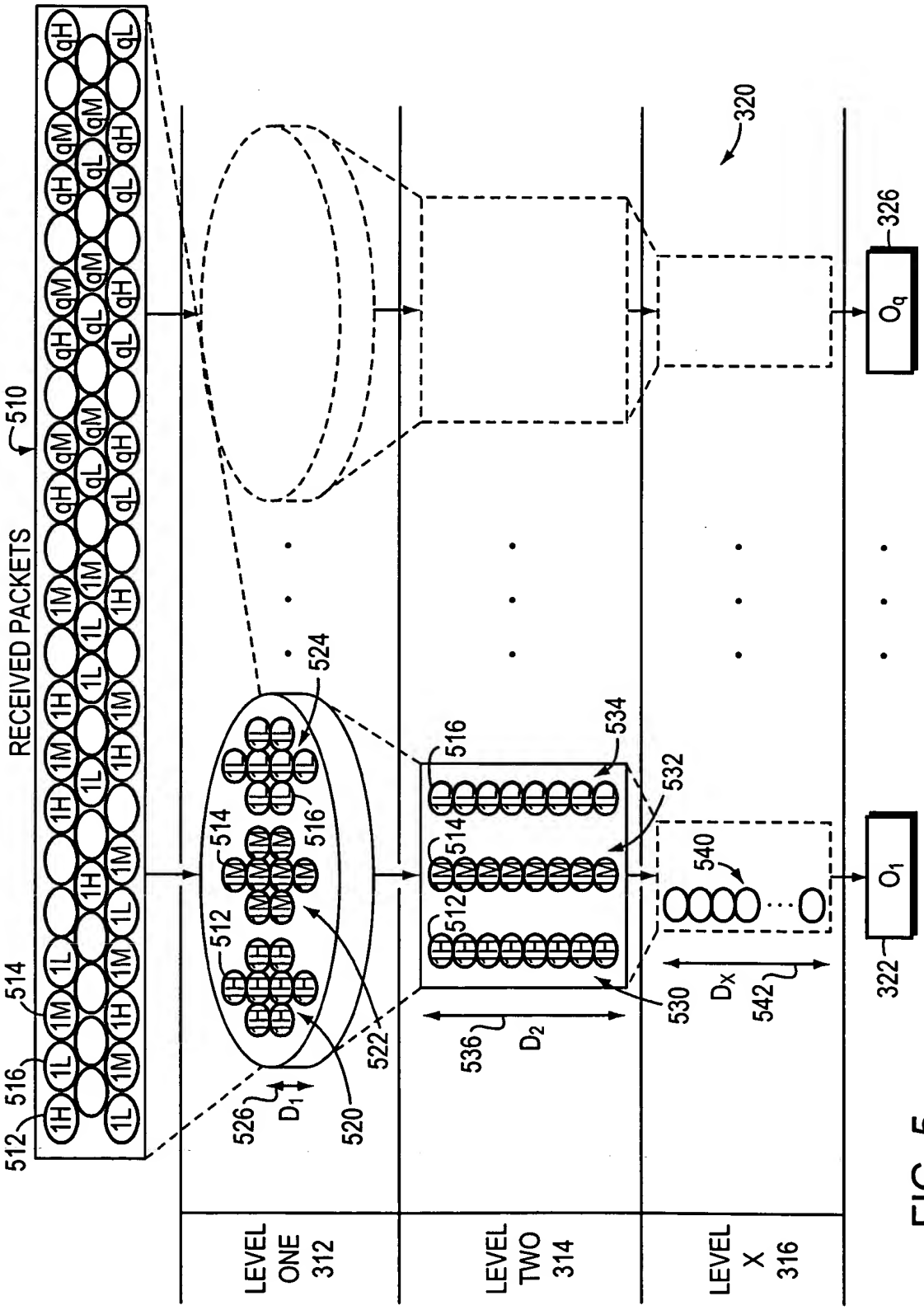
RECEIVED PACKETS
510
514
516
512
524
526
D_1
520
522
536
D_2
530
532
534
540
D_X
542
322
326
320
O_q
O_1
LEVEL ONE 312
LEVEL TWO 314
LEVEL X 316

FIG. 5

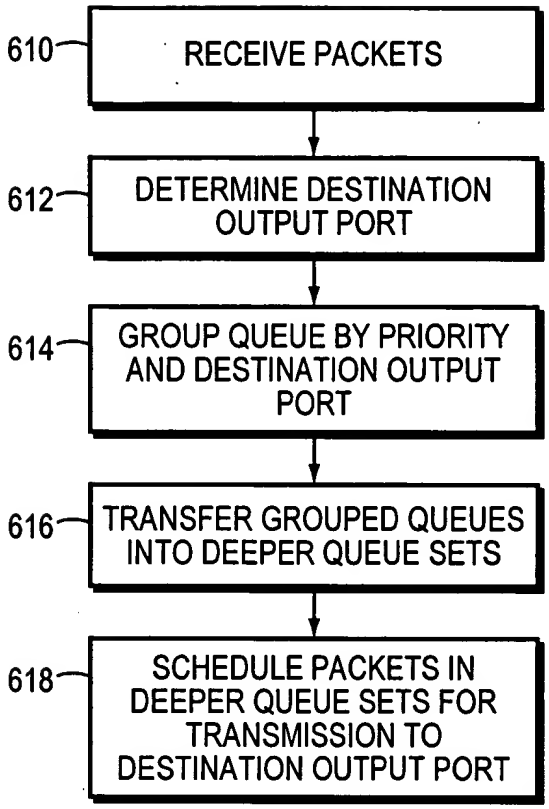
610
RECEIVE PACKETS
612
DETERMINE DESTINATION OUTPUT PORT
614
GROUP QUEUE BY PRIORITY AND DESTINATION OUTPUT PORT
616
TRANSFER GROUPED QUEUES INTO DEEPER QUEUE SETS
618
SCHEDULE PACKETS IN DEEPER QUEUE SETS FOR TRANSMISSION TO DESTINATION OUTPUT PORT

FIG. 6

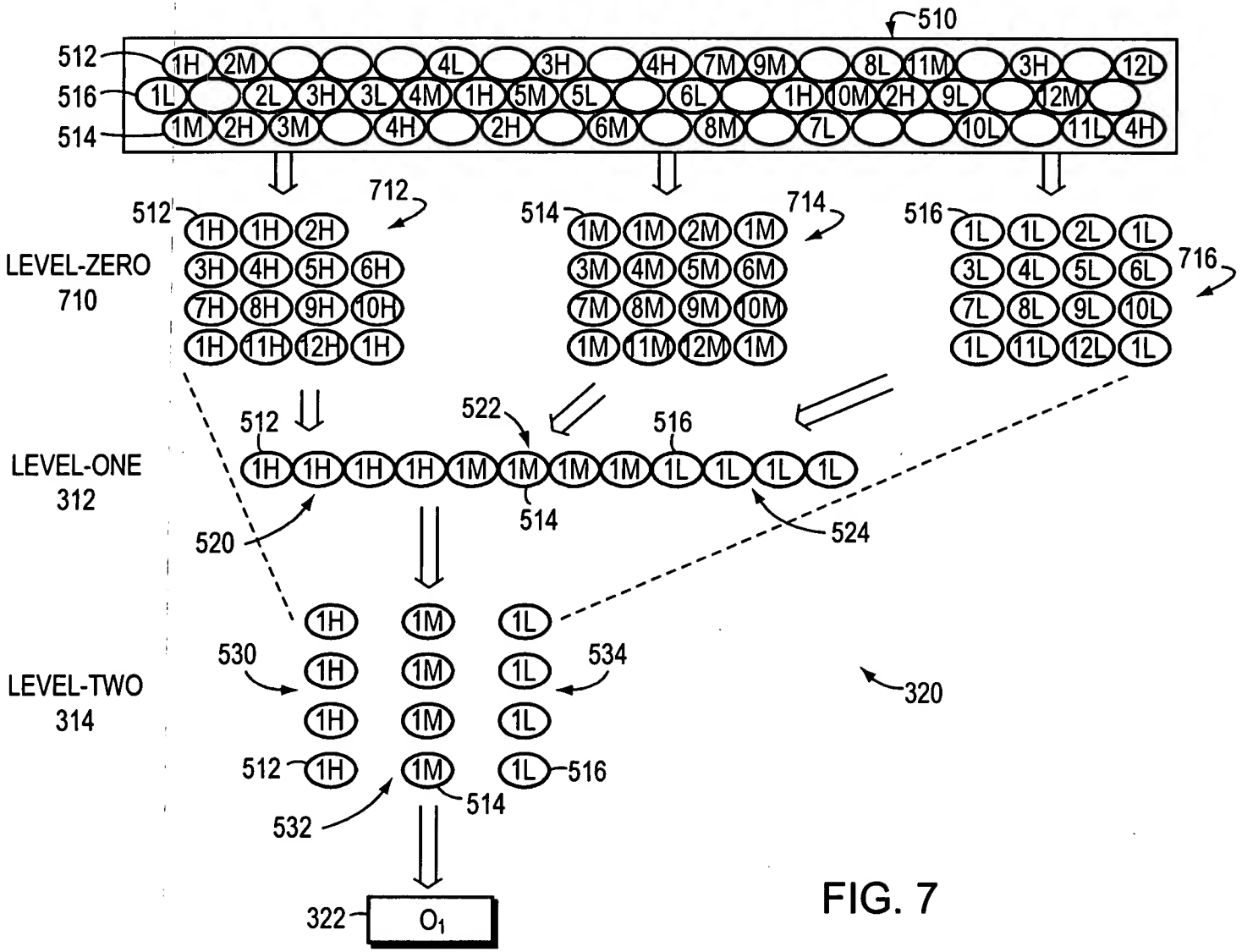
510
512
516
514
1H 2M 4L 3H 4H 7M 9M 8L 11M 3H 12L
1L 2L 3H 3L 4M 1H 5M 5L 6L 1H 10M 2H 9L 12M
1M 2H 3M 4H 2H 6M 8M 7L 10L 11L 4H
712
714
716
LEVEL-ZERO
710
1H 1H 2H
3H 4H 5H 6H
7H 8H 9H 10H
1H 11H 12H 1H
1M 1M 2M 1M
3M 4M 5M 6M
7M 8M 9M 10M
1M 1M 12M 1M
1L 1L 2L 1L
3L 4L 5L 6L
7L 8L 9L 10L
1L 11L 12L 1L
LEVEL-ONE
312
522
520
524
LEVEL-TWO
314
530
534
320
532
322
O_1

FIG. 7

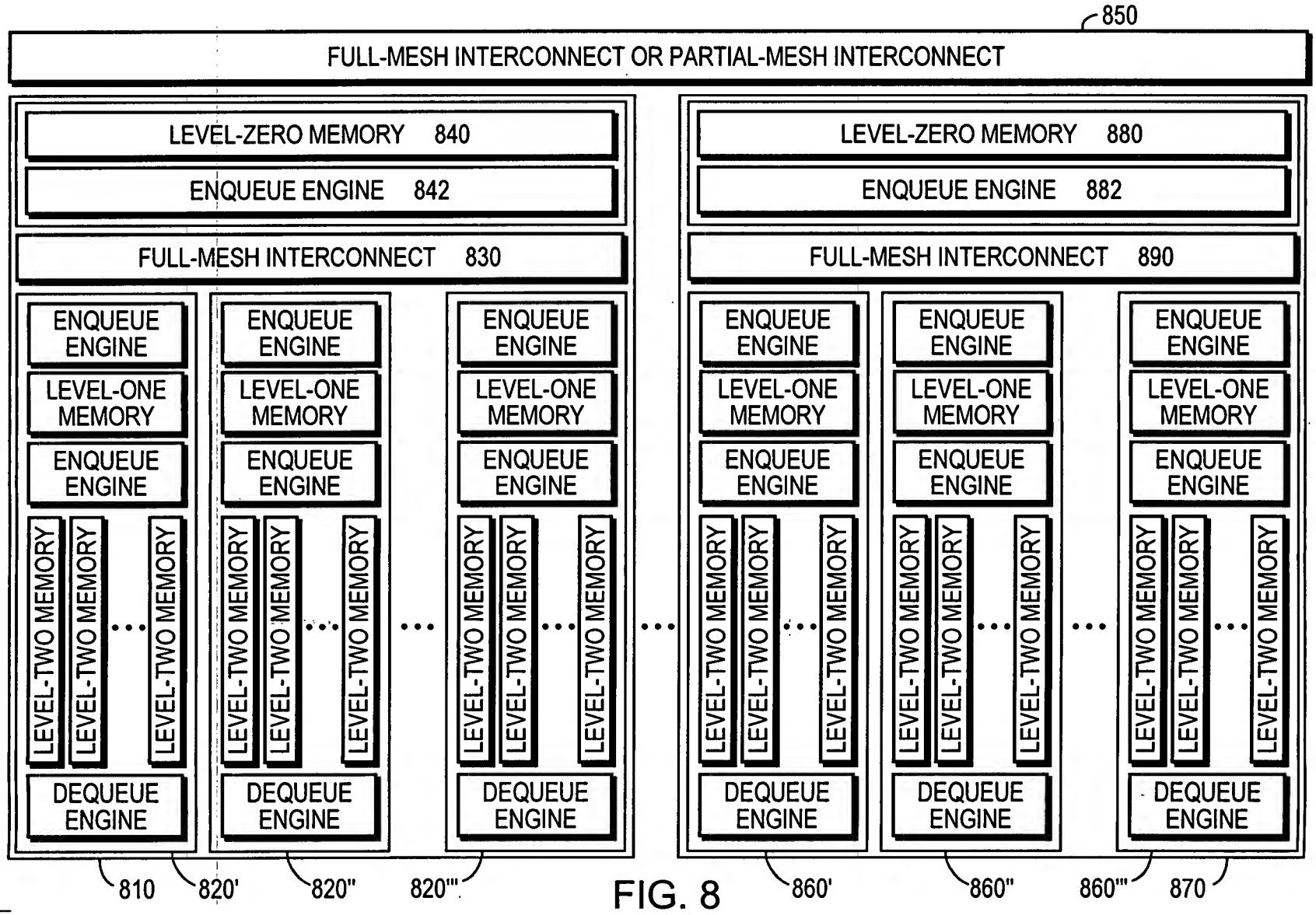
850
FULL-MESH INTERCONNECT OR PARTIAL-MESH INTERCONNECT
LEVEL-ZERO MEMORY 840
ENQUEUE ENGINE 842
FULL-MESH INTERCONNECT 830
LEVEL-ZERO MEMORY 880
ENQUEUE ENGINE 882
FULL-MESH INTERCONNECT 890
ENQUEUE ENGINE
LEVEL-ONE MEMORY
ENQUEUE ENGINE
LEVEL-TWO MEMORY
DEQUEUE ENGINE
810
820'
820"
820'"
860'
860"
860'"
870

FIG. 8